RTL8192EU-CG

SINGLE-CHIP 802.11b/g/n 2T2R WLAN USB 2.0 CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2012/12/1	Preliminary release

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1. General Description

The Realtek RTL8192EU is a highly integrated single-chip MIMO (Multiple In, Multiple Out) Wireless LAN (WLAN) solution for the wireless high throughput 802.11n specification. It combines a MAC, a 2T2R capable baseband, and RF in a single chip. The RTL8192EU provides a complete solution for a high throughput performance wireless Lan controller

The RTL8192EU baseband implements Multiple Input, Multiple Output (MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with 2 transmit and 2 receive paths (2T2R) and is compatible with the 802.11n specification. Features include two spatial streams transmission, short Guard Interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth. The RTL8192EU provides a spatial stream Space-Time Block Code (STBC), Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) encoding and decoding to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to two antennas. As the recipient, the RTL8192EU also supports explicit sounding packet feedback that helps senders with beamforming capability. With two independent RF blocks, the RTL8192EU can perform fast roaming without link interruption.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available along with complementary code keying to provide data rates of 1, 2, 5.5 and 11Mbps with long or short preamble. The high-speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provides the maximum data rate of 54Mbps and 300Mbps for 802.11g and 802.11n MIMO OFDM respectively.

The RTL8192EU builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with maximal-ratio-combine (MRC) applying up to 2 receive paths are implemented. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference. Receive vector diversity for multi-stream application is implemented for efficient utilization of MIMO channels. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for radio frequency front-end impairments. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8192EU supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain the better performance in the analog portions of the transceiver.

The RTL8192EU MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The RTL8192EU provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 56-pin QFN
- CMOS MAC, Baseband MIMO PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n MIMO solution for 2.4GHz band
- 2x2 MIMO technology for extended reception robustness and exceptional throughput
- Maximum PHY data rate up to 144.4Mbps using 20MHz bandwidth, 300Mbps using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating at 802.11n data rates

Host Interface

- Complies with USB Specification Revision 2.0
- USB bridge for RTL8761 Bluetooth connection

Standards Supported

- 802.11e QoS Enhancement (WMM, WMM-SA Client mode)
- 802.11h TPC, Spectrum Measurement
- 802.11k Radio Resource Measurement
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8192EU to assume multiple MAC identities when used as a wireless bridge
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

Peripheral Interfaces

- General Purpose Input/Output (16 pins)
- Three configurable LED pins
- Configurable Bluetooth Coexistence Interface

PHY Features

- 802.11n MIMO OFDM
- Two Transmit and Two Receive path (2T2R)
- 20MHz and 40MHz bandwidth transmission

- Short Guard Interval (400ns)
- Sounding packet
- Low Density Parity Check (LDPC) to enhance link robustness over range
- Transmit Beamforming
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 300Mbps in 802.11n
- OFDM receive diversity with MRC using up to 2 receive paths. Switch diversity used for DSSS/CCK.
- Selectable digital transmit and receive FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

3. Application Diagram

3.1. Single-Band 11n 2x2 WLAN-Only Application

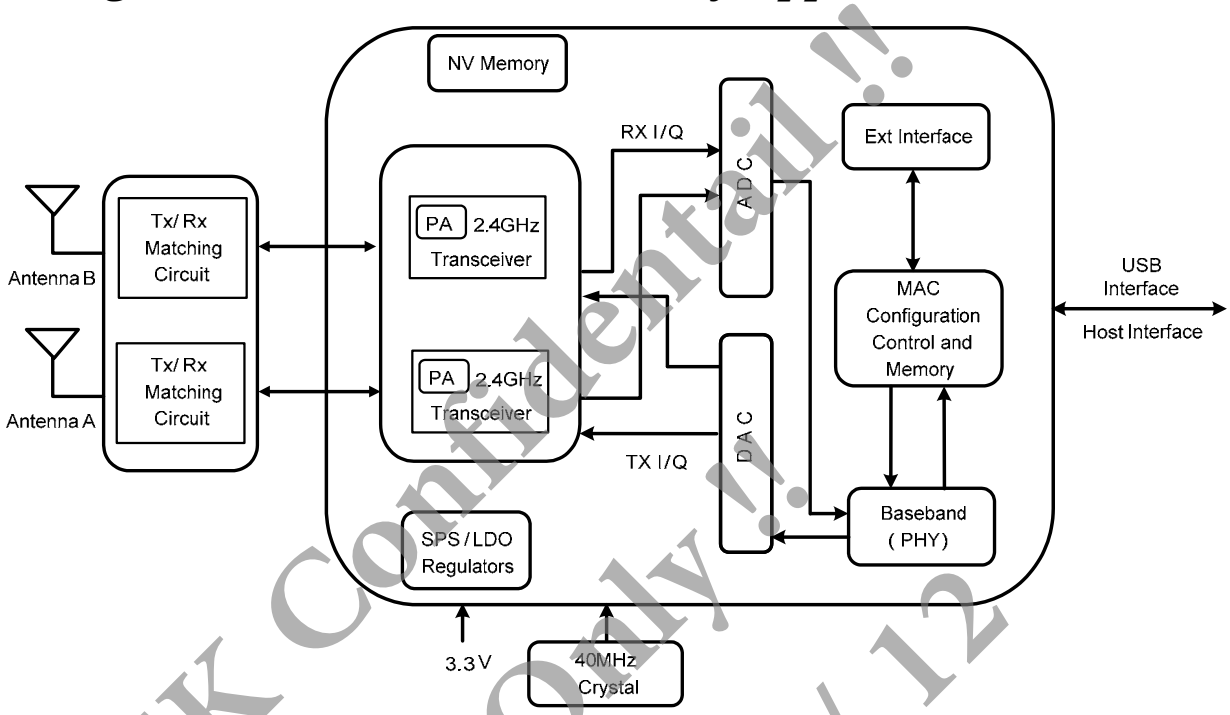


Figure 1. Single-Band 11n (2x2) WLAN Solution

3.2. Single-Band 11n 2x2 WLAN-and-Bluetooth Application

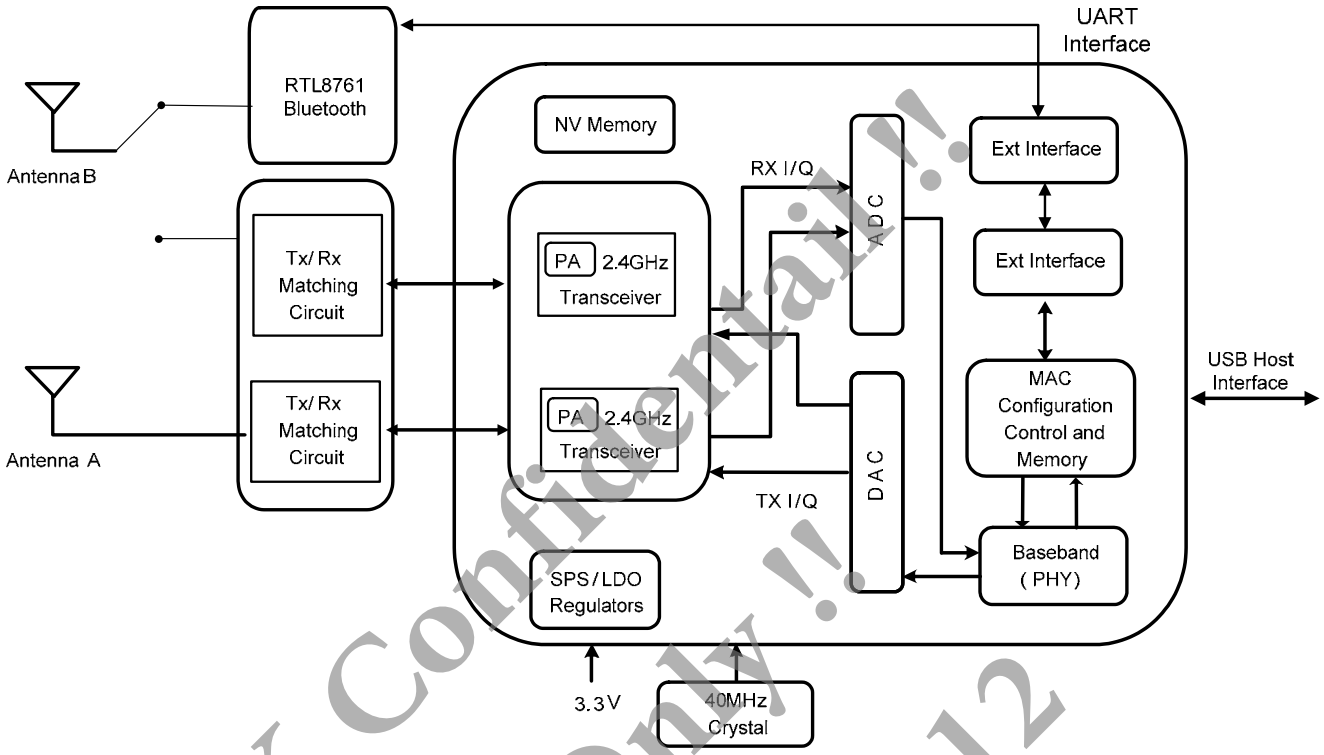


Figure 2. Single-Band 11n (2x2) WLAN and Bluetooth Solution

4. Pin Assignments

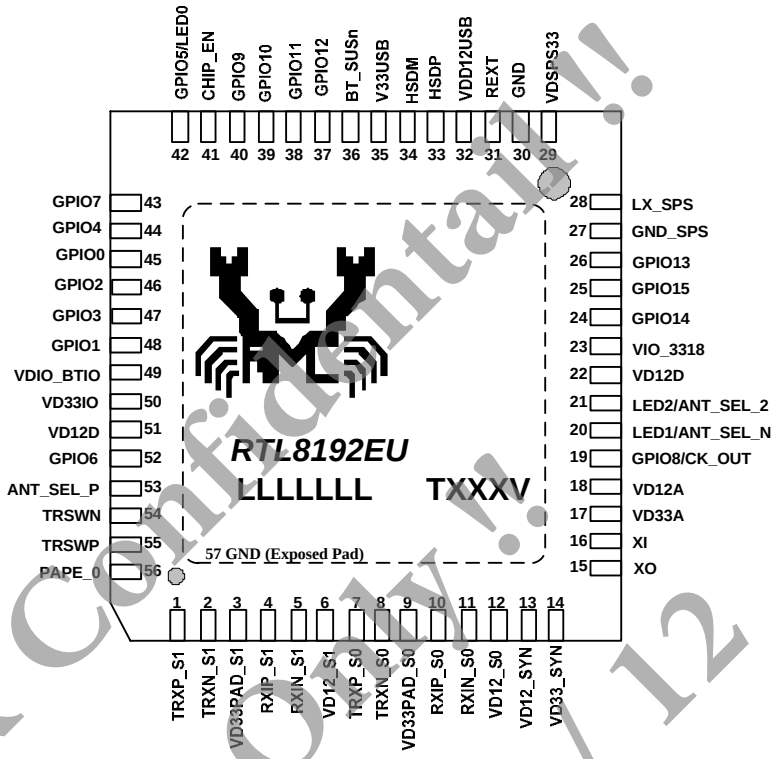


Figure 3. Pin Assignments

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 3.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input	O: Output
T/S: Tri-State bi-directional input/output pin	S/T/S: Sustained Tri-State
O/D: Open Drain	P: Power pin

5.1. Power-On Trap Pins

Table 1. Power On Trap Pins

Symbol	Type	Ball No	Description
TEST_MODE_SEL	I	52	Shared with GPIO6 0: Normal operation mode 1: Enter into test/debug mode
SPS_LDO_SEL	I	48	Shared with GPIO1 0: Internal switching regulator select 1: Internal LDO select
XTAL_SEL0	I	40	Shared with GPIO9 0: 40MHz clock source 1: 25MHz clock source

5.2. USB Transceiver Interface

Table 2. USB Transceiver Interface

Symbol	Type	Pin No	Description
HSDP	IO	33	High-Speed USB D+ Signal
HSDM	IO	34	High-Speed USB D- Signal

5.3. Power Pins

Table 3. Power Pins

Symbol	Type	Pin No	Description
LX_SPS	P	28	Switching Regulator Output
VD33PAD_S1, VD33PAD_S0, VD33_SYN, VD33A	P	3,9,14,17	VDD 3.3V for Analog Input
VIO3318, VDSPS33, V33USB, VDIO_BTIO, VD33IO,	P	23, 29,35,49,50	VDD 3.3V for Digital Input
VD12_S1, VD12_S0, VD12A, VDD12USB	P	6,12,13,18,31	Analog 1.2V Regulator Input
VD12D	P	22,51	Digital 1.2V Regulator Input
GND_SPS, GND, GND	P	27,30,57	Ground

5.4. RF Interface

Table 4. RF Interface

Symbol	Type	Pin No	Description
TRSWN	O	54	Transmit/Receive Signal
TRSWP	O	55	Transmit/Receive Signal
PAPE_0	O	56	2.4GHz Transmit Power Amplifier Power Enable 0
TRXP_S0	O	7	RF TX_S0 Negative Signal
TRXN_S0	O	8	RF TX_S0 Positive Signal
RXIP_S0	I	10	RF RX_S0 Positive Signal
RXIN_S0	I	11	RF RX_S0 Negative Signal
TRXP_S1	O	1	RF TX_S1 Negative Signal
TRXN_S1	O	2	RF TX_S1 Positive Signal
RXIP_S1	I	4	RF RX_S1 Positive Signal
RXIN_S1	I	5	RF RX_S1 Negative Signal
ANT_SEL_P	O	53	Antenna Control Positive Signal
ANT_SEL_N	O	20	Antenna Control Negative Signal Shared with LED1, can be selected by control register
ANT_SEL_2	O	21	Antenna Control Extend Signal Shared with LED2, can be selected by control register

5.5. PTA Interface

Table 5. PTA Interface

Symbol	Type	Pin No	Description
WL_ACT	IO	45	Bluetooth Coexistence WL_ACT Pin The WL_ACT signal indicates when the WLAN is either transmitting or receiving in the 2.4GHz ISM band. Shared with GPIO0 , can be selected by control register
BT_STATE	IO	46	Bluetooth Coexistence BT_STAT Pin. The BTSTAT signal indicates when normal Bluetooth packets are being transmitted or received. Shared with GPIO2, can be selected by control register
BT_PRI	IO	47	Bluetooth Coexistence BT_PRI Pin. The BT_PRI signal indicates when a high priority Bluetooth packet is being transmitted or received. Shared with GPIO3, can be selected by control register

5.6. LED Interface

Table 6. LED Interface

Symbol	Type	Pin No	Description
LED0	O	42	LED Pins (Active Low) Shared with GPIO5, can be selected by control register
LED1	O	20	LED Pins (Active Low) Shared with ANT_SEL_N, can be selected by control register
LED2	O	21	LED Pins (Active Low) Shared with ANT_SEL_2, can be selected by control register

5.7. Clock and Other Pins

Table 7. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	16	OSC Input (default:40Mhz) Input of Crystal clock reference
XO	O	15	Output of Crystal Clock Reference
CHIP_EN	I	41	This Pin can Externally Shutdown RTL8192EU without Extra Power Switch
GPIO0	IO	45	General Purpose Input/Output Pin Shared with ANT_SEL_4 and WL_ACT, can be selected by control register
GPIO1/	IO	48	General Purpose Input/Output Pin.
GPIO2/ BT_STATE	IO	46	General Purpose Input/Output Pin Shared with ANT_SEL_5 and BT_STA, can be selected by control register
GPIO3/ BT_PRI	IO	47	General Purpose Input/Output Pin Shared with ANT_SEL_6 and BT_PRI, can be selected by control register
GPIO4	IO	44	General Purpose Input/Output Pin
GPIO5/LED0	IO	42	General Purpose Input/Output Pin Shared with LED0, can be selected by control register
GPIO6	IO	52	General Purpose Input/Output Pin.
GPIO7	IO	43	This pin can also support WLAN Radio off function with host interface remaining connected.
GPIO8	IO	19	General Purpose Input/Output Pin
GPIO9	IO	40	TGeneral Purpose Input/Output Pin
GPIO10	IO	39	General Purpose Input/Output Pin
GPIO11	IO	38	General Purpose Input/Output Pin
GPIO12	IO	37	General Purpose Input/Output Pin
GPIO13	IO	26	General Purpose Input/Output Pin
GPIO14	IO	24	General Purpose Input/Output Pin
GPIO15	IO	25	General Purpose Input/Output Pin

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 8. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 9. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33A, VD33PAD_S0, VD33PAD_S0, VD33_SYN, VDSPS33, V33USB, VDIO_BTIO, VD33IO	3.3V Supply Voltage	3.0	3.3	3.6	V
VD12A, VD12D, VD12_S0, VD12_S1, VDD12USB	1.2V Core Supply Voltage	1.10	1.2	1.32	V
IDD33	3.3V Rating Current	-	-	600	mA

6.2.2. Digital IO Pin DC Characteristics

Table 10. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

Table 11. 1.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.7	1.8	2.0	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	1.62	--	1.8	V
V_{OL}	Output low voltage	0	--	0.18	V

7. USB Bus during Power On Sequence

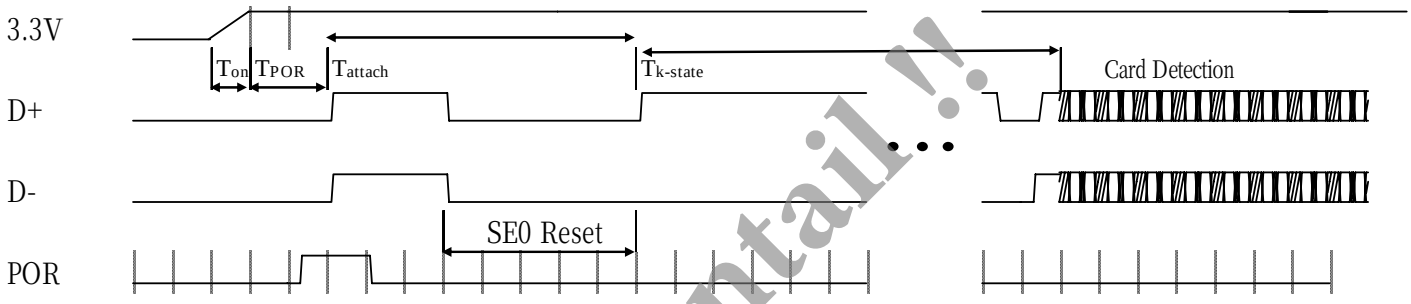


Figure 4. RTL8192EU USB Bus Power On Sequence

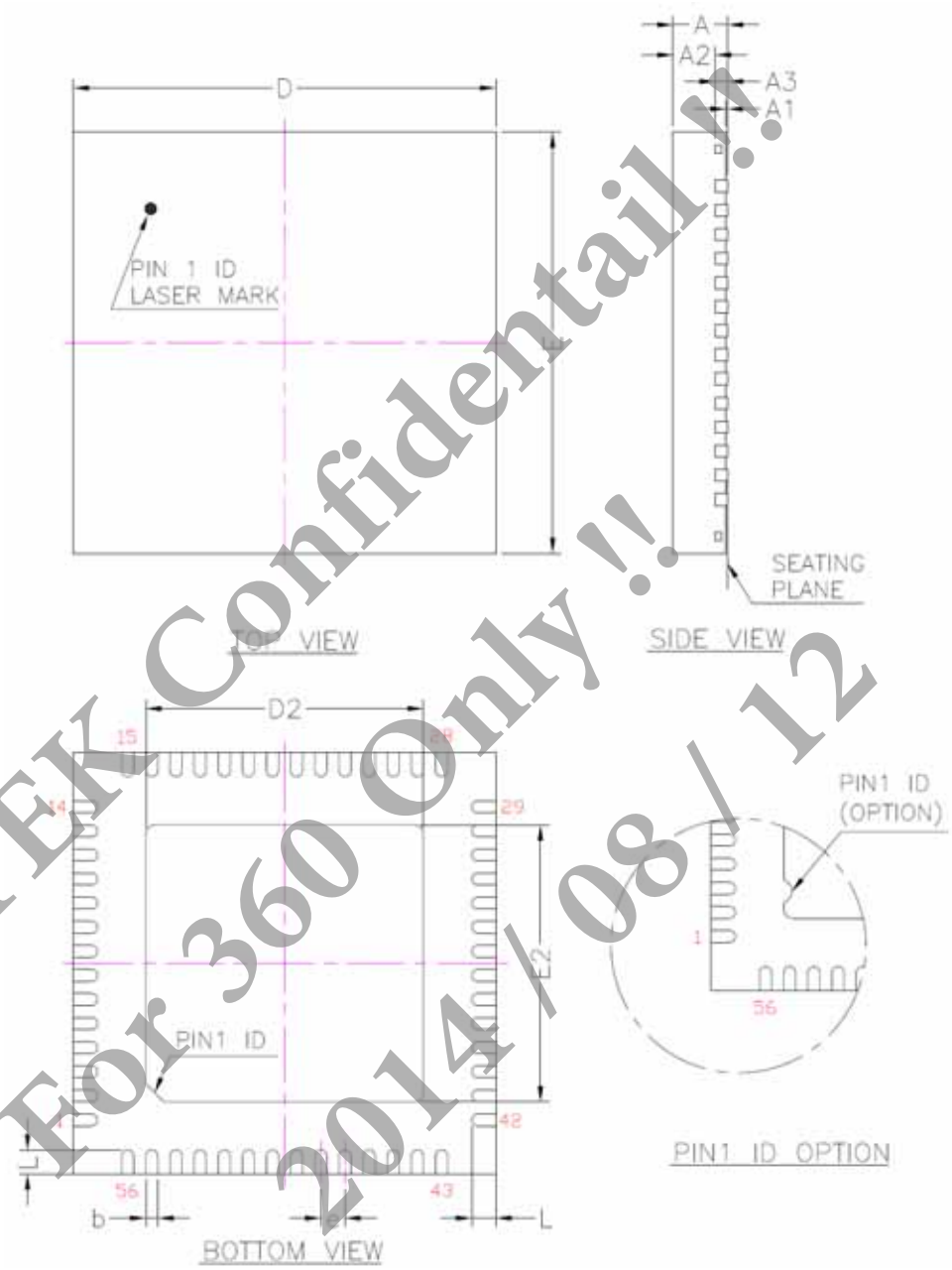
T_{on}: The main power ramp up duration
T_{por}: The power on reset releases and power management unit executes power on tasks
T_{attach}: USB attach state
$T_{k\text{-}state}$: the duration from resister attached to USB host starting card detection procedure

The power on flow description:
After main 3.3V ramp up, the internal power on reset is released by power ready detection circuit and the power management unit will be enabled. The power management unit enables the internal regulator and clock circuits.
The power management unit also enables the USB circuits.
USB analog circuits attach resisters to indicate the insertion of the USB device

Table 12. The typical timing range

	Unit	Min	Typical	Max
T_{on}	ms	--	1.5	5
T_{por}	ms	--	2	10
T_{attach}	ms	2	7	15
$T_{k\text{-}state}$	ms	50	250	--

8. Mechanical Dimensions



8.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	---	0.65	0.70	---	0.026	0.028
A_3		0.2 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		7.00 BSC			0.276 BSC	
D_2/E_2	4.35	4.60	4.85	0.171	0.181	0.191
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

9. Ordering Information

Table 13. Ordering Information

Part Number	Package	Status
RTL8192EU-CG	QFN-56, 'Green' Package	Engineering Samples

Note: See page 7 for package identification.

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